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Reliable Wake-up Receiver with Increased Sensitivity using Low-Noise Amplifiers

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Note: This is the manuscript version of this publication. See https://doi.org/10.1109/SSD54932.2022.9955764 for the published version. Current version: March 4, 2024.

Abstract

For power-limited wireless sensor networks, energy efficiency is a critical concern. Receiving packets is proven to be one of the most power-consuming tasks of a wireless sensor node. Wake-up receivers enable asynchronous communication while maintaining low power consumption. Recent wake-up receiver designs have low sensitivity, high power consumption, or lack of reliability and reproducibility. The proposed receiver circuit utilizes a two-stage low-noise amplifier to achieve a sensitivity of −80 dBm. A duty-cycling approach was introduced to reduce the average power consumption to 14.2 µW. The reliability of the proposed design was ensured by introducing a special low-frequency modulation scheme. The reproducibility of the design was ensured by only using commercial off-the-shelf components.

Keywords

wake-up receiver (WuRx), wireless sensor network (WSN), ultra-low power (ULP), low-noise amplifier, envelope detector, schottky diode, operational amplifier, comparator, fast settling, on-demand communication

1 Introduction

The use of batterie-powered and wireless sensor nodes inside large wireless sensor networks (WSNs) is steadily increasing. Powering sensor nodes using small batteries is often mandatory in many applications. Therefore decreasing the node's power consumption is necessary. Latency, transmission range, and sensitivity are significant parameters.

Continuous or real-time wireless communication is essential for many applications creating a WSN. Maintaining continuous wireless communication and ensuring low latency leads usually to a power consumption greater than 10 mW even with modern wireless transceivers. Decreasing the receiving intervals is needed to power a sensor node for a long time with a battery, but increases the latency and response time of the whole WSN.
A wake-up receiver (WuRx) is a special RF receiver, enabling the battery-powered sensor node to be in a continuous receiving mode. The mean power consumption of a WuRx is typically kept below 10 µW and very low latency is assured. The wake-up receiver is connected to a second antenna or RF path of the sensor node. Special wake-up packets (WuPts) need to be transmitted by a so-called wake-up transmitter (WuTx) to signal the wake-up. Inside the WuPt an address can be introduced, ensuring only one sensor node of the network is woken up.
WuRx implementations are divided into two categories: application-specific integrated circuit (ASIC)-based WuRx and WuRx implemented using commercial off-the-shelf (COTS) components [Piy+17]. This publication will focus on the COTS implementation of WuRx. Figure 1 shows the typical building blocks of a COTS WuRx.

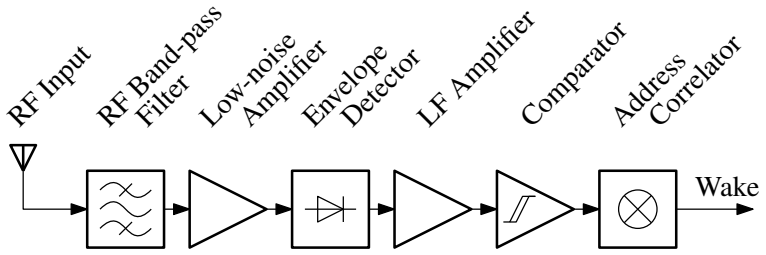

Figure 1: Building blocks of a typical COTS WuRx with low-noise RF amplifier and passive envelope detector.

The WuRx's input signal is characterized by low amplitude, high noise figure, and various interferences. An RF band-pass filter is used to decrease off-band interferences. To further boost the RF signal and increase the signal-to-noise ratio a low-noise amplifier (LNA) is introduced. A passive envelope detector performs the signal detection and conversion to an LF signal. The LF signal needs to be amplified further to be detectable by the following comparator circuit, performing the analog-to-digital conversion. A digital address correlator can be added to implement addressing capabilities of the WuRx and avoid false wake-ups.

2 Related Work

One of the first WuRx designs only utilizing COTS components is [Gam+10]. This design was based on an envelope detector circuit with a Greinacher voltage double followed by the AS3932 as an integrated amplifier, quantifier, and address correlator. A sensitivity of −52 dBm with a current consumption of only 2.78 µA was reached.
This design was further improved by [BD15]. An AS3933 was utilized instead of AS3932 and the envelope detector's LF signal was further amplified, by a power-gated operational amplifier (OA) circuit. An ultra-low-power carrier-detection circuit is implemented, only enabling the OA, when an RF carrier is detected. The sensitivity improved to −60 dBm and the current consumption increased only slightly to 3 µA.
The publication of [Mag+16] introduced the utilization of comparators to digitalize the envelope detector's LF signal. The address matching is implemented inside a microcontroller. Also, an adaptive reference generator using a low-pass filter on the LF signal was introduced. The performance of different comparator types was investigated. The implementation using the comparator LPV7215 reached a sensitivity of −55 dBm while only consuming 1.2 µW.
The approach presented in [Kaz+21] introduced an OA circuit between envelope detector and comparator circuit. This allowed increasing the circuit's sensitivity down to −70 dBm, while remaining a low current consumption of 580 nA. This is possible due to a slow data rate of approximately 20 bit/s, resulting in long WuPts and high latency.
The sensitivity of these WuRx implementations is mainly limited by the noise figure of the envelope detector. No implementations using a passive envelope detector were able to reach a sensitivity beyond −60 dBm while maintaining a fast data rate. To further increase the WuRx's sensitivity, a pre-amplification of the RF signal is needed.
The utilization of an LNA is introduced in [PWK18]. The MAX2643 amplifies the RF signal with 17 dB and the current consumption is 5.3 mA. A high data rate of 250 kbit/s is utilized to keep the active times as short as possible. A duty-cycling is introduced with an active time of 10 ms every 1 s is used. This leads to an average current consumption of 5.7 µA. A sensitivity of −71 dBm was achieved.
The LNA-based design from [BDK18] utilizes bipolar junction transistor (BJT)-based LNA and LF amplifier. The LNA amplifies 36 dB while only consuming 550 µA. A comparator circuit is used to digitalize the LF amplifier's output. A special communication scheme is introduced capable of supporting a duty-cycled

receiver. Low active current consumption of only 1.3 mA and fast settling times enable the WuRx to stay active for only 55 µs every 32 ms. The average power consumption is 3 µW while sensitivity is –90 dBm.
Further improving the implementation of [BDK18], regarding average power consumption and sensitivity, is not the goal of this publication. Because of the utilization of a custom BJT-based LNAs, working in the sub-milliampere range, experimental results are very hard to reproduce. COTS LNAs are used in our proposed circuit, at the cost of a gain reduction and higher current demand. Further problems within the communication scheme of [BDK18] were detected, leading inevitably to a random packet loss. This publication introduces a special low-frequency modulation and measurements were made to ensure no random packet loss occurs. This way the overall reliability and reproducibility of the WuRx implementation was heavily increased.

3 Building Block Analysis

The following section focuses on the component analysis and selection to propose a design of an LNA-based WuRx, working in the 868 MHz frequency band. Duty-cycling will be utilized to decrease the average current consumption. Ensuring low settling times of all components is essential.

3.1 RF Band-pass Filter

The introduction of an RF band-pass filter is necessary to ensure good WuRx's immunity to interferences from other RF bands. Antenna's, LNA's, and matching circuit's frequency responses are band-pass shaped but do not offer a narrow-band response. Introducing a surface acoustic wave (SAW) filter into the WuRx design significantly reduces interferences but introduces an additional insertion loss.
The utilized SAW filter B39871B3725U410 has a center frequency of 869 MHz, a bandwidth of 2 MHz, and a typical insertion loss of 2.5 dB [RF319]. This insertion loss directly decreases the WuRx's sensitivity, when compared to an ideal system, but the utilization of a SAW filter in a noisy real-live environment is essential.

3.2 Low-noise Amplifier

This work focuses on the utilization of the MAX2640 COTS LNA [Max15]. The MAX2640 was selected because of its low current consumption of 3.5 mA and high

gain of 14.4 dB. A single-stage design according to Figure 2 and the datasheet [Max15] was built up.

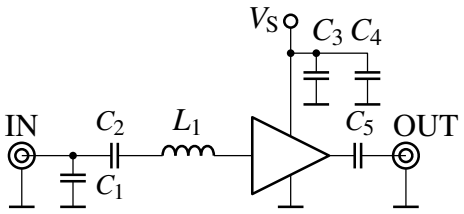

Figure 2: Schematic of the low-noise amplifier utilizing the MAX2640, based on [Max15].

With a supply voltage of 3.3 V, the LNA showed a current consumption of 3.19 mA. Connecting the test printed circuit board (PCB) to a two-port network analyzer delivered the following S-parameters at 868 MHz: $S_{11} = -20$ dB, $S_{21} = 14$ dB, $S_{12} = -30$ dB, $S_{22} = -15$ dB.
Measuring the settling time of the LNA circuit showed a long duration of 7.5 µs. Decreasing the capacitance of C_1 from 470 pF to 10 pF and matching the circuit, decreases the settling time to 420 ns.
For the proposed WuRx circuit, a dual-stage LNA design is used. The total current consumption was measured with 6.7 mA and the S-parameters of the whole circuit are measured as following: $S_{11} = -13.3$ dB, $S_{21} = 27.6$ dB, $S_{12} = -33$ dB, $S_{22} = -15.1$ dB.

3.3 Impedance Matching and Envelope Detector

Utilizing a Greinacher voltage doubler configuration as an envelope detector circuit is common in recent publications [Gam+10; BD15; Mag+16; Kaz+21; BDK18]. Impedance matching is necessary to match the 50 Ω output impedance of the LNA to the envelope detector's load impedance. A matching circuit with two lumped components is used, based on the publications [Gam+10; Mag+16; Kaz+21; BDK18]. Figure 3 shows the schematic of the envelope detector.

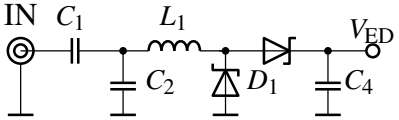

Figure 3: Schematic of the envelope detector utilizing a Greinacher voltage doubler.

The diode HSMS-2852 from Agilent Technologies is the typical diode used in the envelope detector by many publications [BD15; Mag+16; BDK18; Kaz+21]. Because this diode is not provided anymore by the manufacturer, an alternative is needed. The SMS7630-006LF from Skyworks Solution Inc. has nearly identical

parameters and previous investigations were made [FSD21], to ensure that the diode SMS7630 is a good alternative.
Below the input power of around −30 dBm, the diode behaves according to (1) with V_{ED} the envelope detector output voltage, γ^{OC} the open-circuit voltage sensitivity, and P_{in} the RF input power [BB03, p. 569].

$$V_{ED} = \gamma^{OC} \cdot P_{in} \tag{1}$$

The diode's LF behavior can be modeled as a voltage source with series resistance, so-called video resistance R_v. R_v is defined by the diode's series resistance R_s and junction resistance R_j, see (2) [BB03, p. 569].

$$R_v = R_s + R_j \tag{2}$$

Voltage sensitivity and video resistance were determined experimentally for the setup described in Figure 3. The envelope detector output voltage was measured for different RF powers. Figure 4 shows the measurements results.

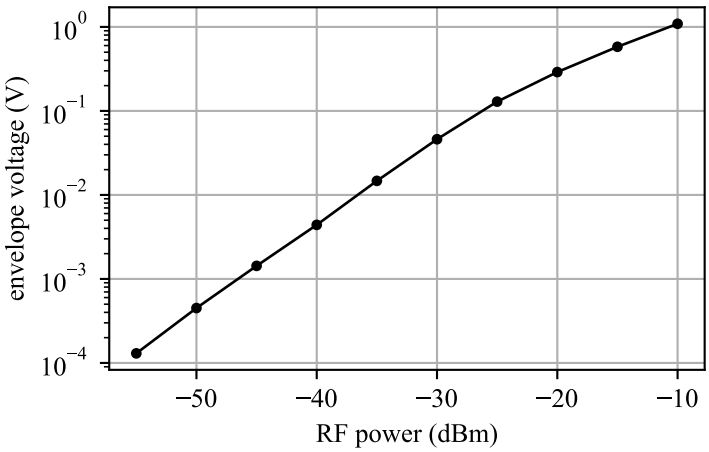

Figure 4: Results of the voltage sensitivity measurement.

The figure shows clearly the square-law behavior of the envelope detector for input levels lower than −30 dBm. The voltage sensitivity resulting into $\gamma^{OC} = 45\,\mathrm{mV/\mu W}$.
To measure the video resistance, a load resistor was added. When adding a 10 kΩ resistor, envelope voltage output drops from 44.1 mV to 21.7 mV. The video resistance can be calculated to 11.7 kΩ.
The video resistance forms together with C_4 a low-pass filter. The filter's cut-off frequency has to be selected accordingly, so that RF components are appropriately removed, but the LF signal is not disturbed. With $C_4 = 10\,\mathrm{pF}$ a cut-off frequency

of 1.6 MHz can be estimated according to (3).

$$f_C = \frac{1}{2\pi \cdot R_v \cdot C_4} \tag{3}$$

3.4 LF Amplifier Circuit

Reference [BDK18] utilized a BJT-based amplifier. Because DC-blocking capacitors needed for the BJT amplifier, the LF signal is high-pass filtered. The high-pass filter time constant has to be set accordingly, so that the signal is not disturbed and a fast settling time is ensured. Non-inverting OA-based amplifiers do not rely on DC blocking capacitors.
A COTS OA device is selected according to current consumption, gain-bandwidth product (GBWP) and rail-to-rail capabilities. The TSV6391A was selected and is offering GBWP of 2 MHz and current consumption of typically 50 µA [STM15].
The input offset voltage of the OA limits the minimum detectable signal. A value of ±500 µV at room temperature is given by the datasheet [STM15]. With an envelope detector voltage sensitivity of $\gamma = 45\,\mathrm{mV/\mu W}$, a signal level of only –50 dBm can be detected. That is why a biasing circuit needs to be introduced to add a DC voltage to the envelope detector output signal. Figure 5 shows the utilized amplification circuit with the LF equivalent circuit of the envelope detector.

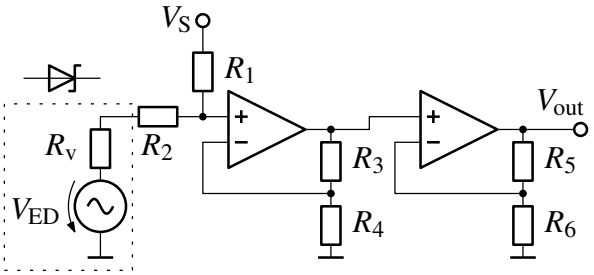

Figure 5: Schematic of the LF amplifier circuit with envelope detector equivalent circuit, biasing circuit, and dual-stage OA circuit, based on [Tex01].

The envelope detector is replaced by its Thévenin equivalent circuit. The biasing circuit is formed through the voltage divider of R_1, the series resistance of R_2, and diode's video resistance R_V. The biasing voltage was selected to around 3 mV by setting $V_S = 3.3\,\mathrm{V}$, $R_1 = 10\,\mathrm{M\Omega}$, and $R_2 = 0$.
A dual-stage amplifier design was utilized to increase gain and bandwidth. The feedback resistors R_3 to R_4 were selected to create an amplification factor of 14 per stage, resulting in a total gain of around 200 and a bandwidth of 170 kHz.

3.5 Comparator Circuit

A COTS comparator needs to be selected according to the current consumption and propagation delay. Low propagation delay allows fast signal transmissions and fast settling time. The comparator's input offset voltage and hysteresis limit the minimum detectable signal. The TLV3201 is selected because of its low current consumption of 40 µA and low propagation delay of typically 40 ns [Tex16]. The maximum input offset voltage is given to 5 mV at room temperature.

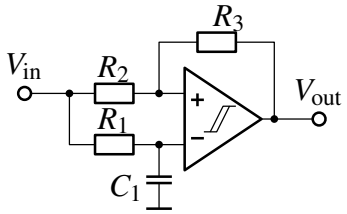

Figure 6: Schematic of the comparator with external hysteresis and adaptive reference generator, based on [Max05].

Figure 6 shows the schematic of the comparator circuit. To compensate for the variations in the input offset voltage an external hysteresis circuit is added by the resistors R_2 and R_3. The hysteresis voltage difference is set to 20 mV.
On the negative input of the comparator, a low-pass filter is added, acting as a data slicer. When a symmetrical square-wave signal is applied the capacitor C_1 charges up to half of the peak-to-peak voltage. The data slicer time constant τ_{DS} is set by the R_1 and C_1 according to (4).

$$\tau_{DS} = R_1 \cdot C_1 \tag{4}$$

Application note [Max05] recommends the dimensioning $\tau_{DS} = 5 \cdot T_{bit}$ with T_{bit} the bit duration. But large τ_{DS} also increases the settling time of the comparator circuit. That is why τ_{DS} was set to 3.3 µs, but T_{bit} is 10 µs. This makes the comparator circuit more susceptible to interferences but ensures a short settling time.

4 Performance Analysis

The proposed circuit, seen in Figure 7, was built up. An MSP430G2553 microcontroller is used to control the components' power supplies and performs the address matching [Tex13].
To evaluate the sensitivity of the WuRx packet error rate (PER) measurements are made. Figure 8 shows the general structure of the PER measurement system, used for the following measurements. A PC is used to control both the frequency

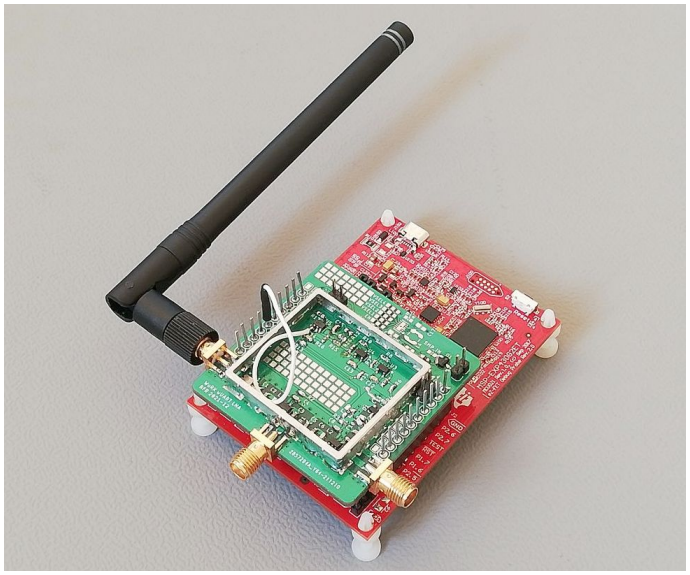

Figure 7: Prototype PCB with MSP430 Launchpad and 868 MHz antenna.

generator and a microcontroller interface. The microcontroller is capable to output the LF signal used by the frequency generator to modulate the WuPt. The RF WuPt is connected to the test circuit. A digital output signal is generated by the test circuit on successful WuPt detection and is fed back into the microcontroller. The microcontroller is capable of counting both transmitted and received packets and can estimate the PER. Varying the frequency generator's output power allows the comparison between different WuRx configurations and setups.

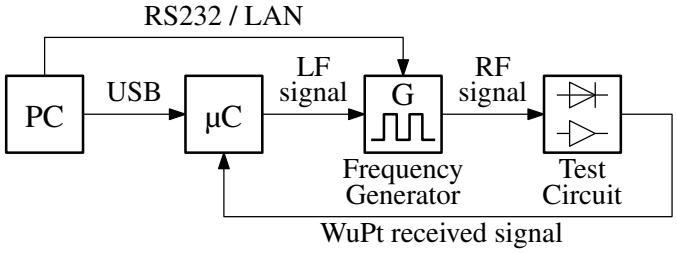

Figure 8: Block diagram of the PER measurement system.

4.1 Steady-state Analysis

Figure 9 shows an oscilloscope measurement with a 50 kHz test signal, modulated onto an 868 MHz carrier with an RF power of −80 dBm. The LF envelope of the test signal can be seen in the first subplot. The second subplot shows the amplifier output. An offset voltage of 780 mV can be seen, which is created by the bias generator, OAs' input offset voltages, and is further amplified. The last subplot shows the comparator output. The successful reconstruction of the test signal can

be seen together with several glitches before and after the signal. These glitches occur due to the low data slicer time constant.

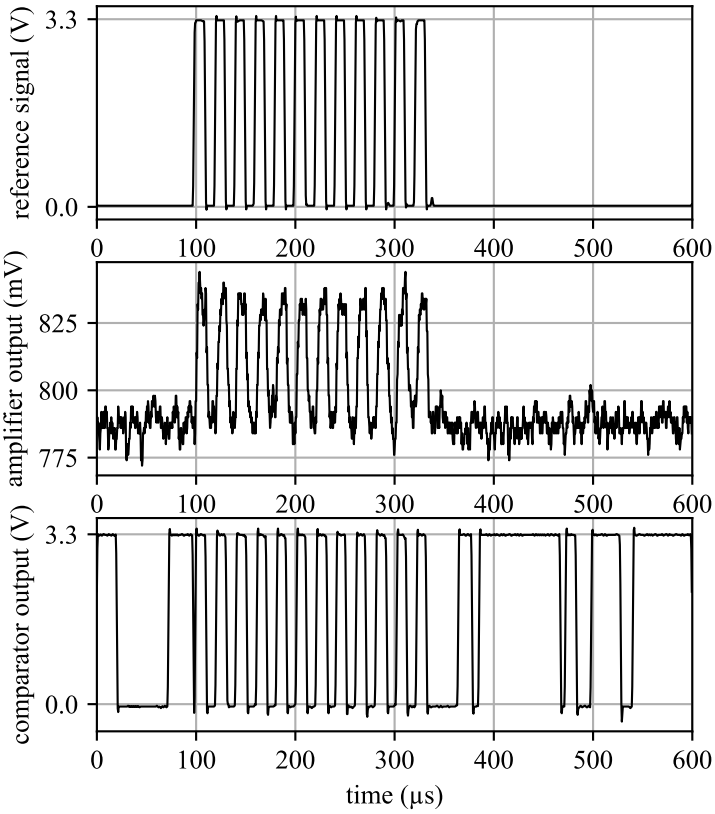

Figure 9: Steady-state oscilloscope measurement with 50 kHz test signal, modulated onto an 868 MHz carrier with an RF power of −80 dBm.

4.2 Duty-Cycling and Circuit Settling

To reduce the average power consumption of the circuit, a duty-cycling approach is introduced. The power supply of the LNA and the LF circuit can be controlled by the MSP430's digital outputs. The WuRx enters the active phase continuously to detect incoming WuPts.

During the active phase, the WuRx needs to detect the presence of a WuPt and extends the active phase accordingly. Keeping the peek time as short as possible is mandatory to reduce WuRx's power consumption.

The peek time is strongly dependent on the data slicer time constant τ_{DS}. Using slower τ_{DS} leads to a longer settling time, until the square-wave signal is seen on the comparator output. The fastest decision method is to measure and compare the time between two consecutive slopes of the comparator output. This method is also used by [BDK18] but is very sensitive to glitches occurring on the comparator output. Sampling the signal and using multiple signal periods to make

this decision would create more reliable results but would increase the peek time drastically.
The minimal suitable peek time was determined experimentally. Multiple peek times and RF input powers were tested. The number of successful signal detections was counted and the results can be seen in Figure 10.

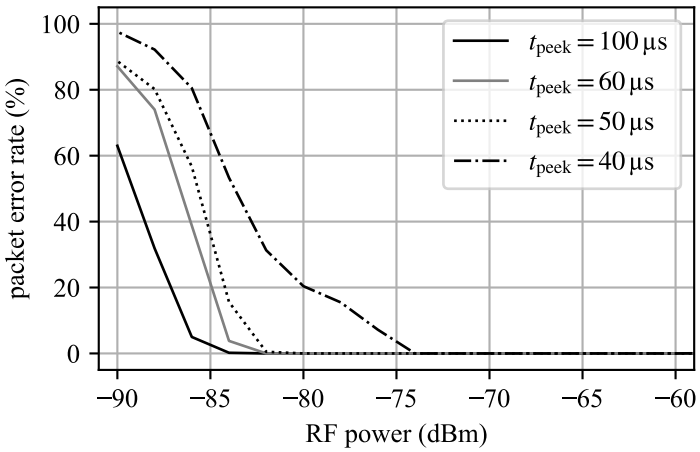

Figure 10: Measurement of successful detected 50 kHz signal at different input powers and for different active phase duration.

With higher peek time the detection of low-power signals becomes more reliable, but also the number of false-positives increases. Using $t_{\text{peek}} = 40\,\mu\text{s}$ results in packet losses starting at –74 dBm. $t_{\text{peek}} = 50\,\mu\text{s}$ was selected as suitable for the application.

4.3 Address Matching

The encoding of an address in the WuPt is essential to avoid false wake-ups. Due to duty-cycling, the WuRx is randomly started during the transmission of the WuPt. Using pauses within the WuPt is not possible, because the WuRx would not be able to detect the presence of a WuPt and no wake-up will occur. The protocol described in [BDK18], shows such pauses and will result in random packet losses.
The idea proposed in this publication is to use an LF frequency modulation (FM) to encode the wake-up address. Because there is always a signal present and no pauses occur, the WuPt detection during the peek time will not fail. Both 50 kHz and 100 kHz square-wave signals will be used to encode binary '1' and '0', respectively. That is done by the microcontroller, measuring continuously the elapsed time between two rising edges of the comparator output.
Figure 11 shows an example WuPt and the decoder's output signal at an RF power

of –75 dBm. The LF reference signal is seen in the first subplot. The second subplot shows the digital output signal of the FM decoding.

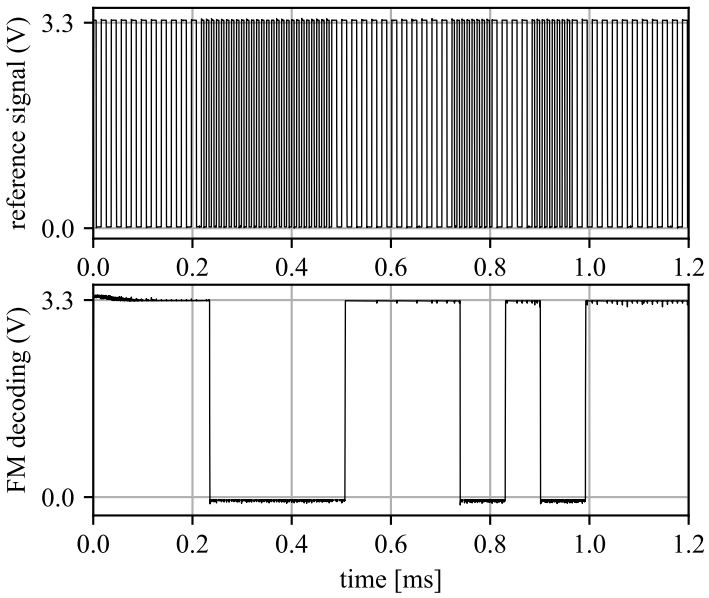

Figure 11: Oscilloscope measurement of address decoding with 50 kHz and 100 kHz test signal at an RF power of –75 dBm.

The FM signal is selected accordingly, that FM decoding output is a valid universal asynchronous receiver transmitter (UART) signal. This signal is fed back into the microcontroller's UART module. Within the UART interrupt address matching can be realized. Currently, only 8 bit addressing is supported.

4.4 Timing

Figure 12 shows the timing diagram for the duty-cycled WuRx communication. t_{peek} is the duration necessary for the WuRx to detect the presence of a WuPt. Due to settling time and data slicer time constant, $t_{\text{peek}} = 50\,\mu\text{s}$ is used. t_{sleep} is the duration between two active phases of the WuRx. Increasing t_{sleep} will decrease the average power consumption of the WuRx, but will increase the transmission time t_{WuPts} and WuTx's current consumption. $t_{\text{sleep}} = 100\,\text{ms}$ will be used for the following analysis. t_{WuPt} is the duration of a single WuPt, transmitting the wake-up address once. The FM-demodulated UART signal has a baud rate of 12.5 kbit/s. The 8-bit address together with start bit, stop bit, and padding lead to a $t_{\text{WuPt}} = 1.36\,\text{ms}$. The address decoding of the WuRx needs to be at least twice t_{WuPt} to ensure the address is received completely, resulting in $t_{\text{addr}} = 2.8\,\text{ms}$. To ensure that WuRx received the address $t_{\text{WuPts}} > t_{\text{sleep}} + t_{\text{addr}}$, resulting in 76 WuPts being transmitted and $t_{\text{WuPts}} = 103.4\,\text{ms}$.

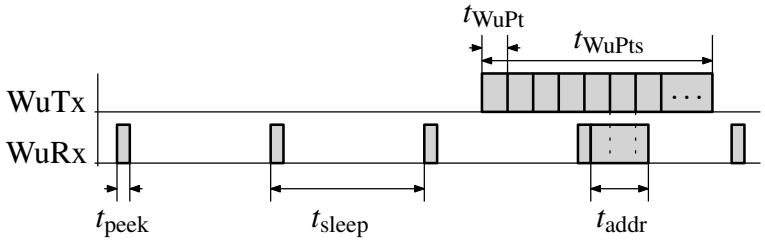

Figure 12: Timing diagram for duty-cycled WuRx communication.

The programming of the MSP430G2553 microcontroller is done using multiple timers. The first timer uses an ultra-low-power crystal oscillator, generating an interrupt every t_{sleep}, to activate the WuRx. During the peek interval the second timer is used to measure the duration between two consecutive slopes and generate a timeout signal after t_{peek}. If a valid wake-up signal is detected, the timeout is extended to t_{addr} and the timer is changed to measure the time between two consecutive rising slopes. The FM signal is decoded continuously and fed into the UART module. The UART module generates an interrupt on byte receive. This byte is compared to the 8-bit wake-up address. On successful WuPt reception or timer timeout the WuRx components are turned off again.

4.5 Sensitivity and Current Consumption

The sensitivity was measured with the PER measurement system. A packet count of $N = 1000$ and a power step size of 0.5 dB were used to generate the PER curve shown in Figure 13.

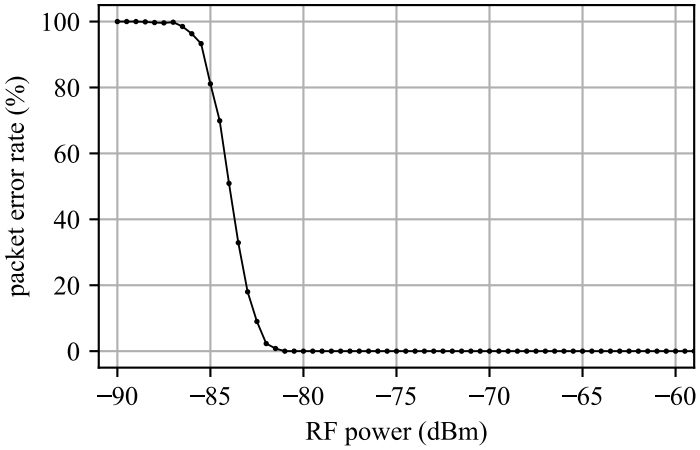

Figure 13: Measurement of the packet error rate of the proposed wake-up receiver.

The proposed WuRx shows a PER below 1 % down to −80 dBm. Down to −86 dBm, WuPts are detectable.

Table 1 shows the current consumption of the proposed WuRx's components. During active phase, the current rises to 7.19 mA. During sleep mode, all WuRx components are deactivated. Only the microcontroller remains active. $t_{\text{peek}} = 50\,\mu\text{s}$ and $t_{\text{sleep}} = 100\,\text{ms}$ results in average current consumption of $\overline{I} = 4.3\,\mu\text{A}$ and average power of $\overline{P} = 14.2\,\mu\text{W}$. The current consumption measured on the prototype is slightly increased, because of the peek period being extended falsely, due to interferences or noise.

Table 1: Proposed Wake-up Receiver's Current Consumption

	Active	**Sleep**
Current Draw (μA)		
LNA	6700	0
LF amplifier	120	0
Comparator	40	0
Microcontroller	330	0.7
Total (μA)	7190	0.7
Duration (ms)	0.05	100
Mean Current Draw (μA)	4.3	
Mean Power (μW)	14.3	

5 Discussion

The proposed circuit shows a way to further improve the sensitivity of wake-up receivers (WuRxs). Using only commercial off-the-shelf (COTS) components, the circuit and the results can be easily reproduced. Biasing circuit, adaptive threshold generator, and hysteresis ensure that this circuit works reliable, even if component characteristics change. Exceptionally making the circuit independent of operational amplifier (OA)'s or comparator's input offset voltage. This makes the circuit more reliable compared to proposed circuits of [BD15; Mag+16; Kaz+21], where circuit's performance strongly varies with component's input offset voltage.

The proposed wake-up packet (WuPt) protocol ensures a reliable WuPt detection during the peek interval. Ensuring no pauses in the WuPt results in a reliable WuPt detection. As shown in Figure 13, the WuRx is capable to detect signals above −80 dBm, and all 1000 test packets were received.

Further work has to be made, to introduce a buck-converter to efficiently use the

circuit with lower supply voltages. Proper circuit performance down to 2 V has to be ensured. The LF circuit has to be further improved to remove false triggers of the comparator and reduce the number of false-wake-ups during the peek interval. Introducing an low-noise amplifier (LNA) with higher gain and lower power consumption shall further improve WuRx's performance.

Acknowledgment

This work is financially supported by Leipzig University of Applied Sciences by funds of Sächsisches Staatsministerium für Wissenschaft, Kultur und Tourismus.

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